

O'zbekistan Respublikasi baylanis, informaciyalastiruv ha'm  
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Tashkent informatsiyaliq texnologiyalari universiteti.

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Kompyuter injiniringi jo'nelisi.

Ornatilgan sistemanin' programmalıq  
ta'miynatin islep shıg'ıw pa'ninen tayarlang'an

# Kurs jumısı

Tema: Aqilli mashina sistemasin jaratiw.



Orınlag'an:

Kalbaeva A

Qabıllag'an:

\_\_\_\_\_

No'kis 2017-jıl

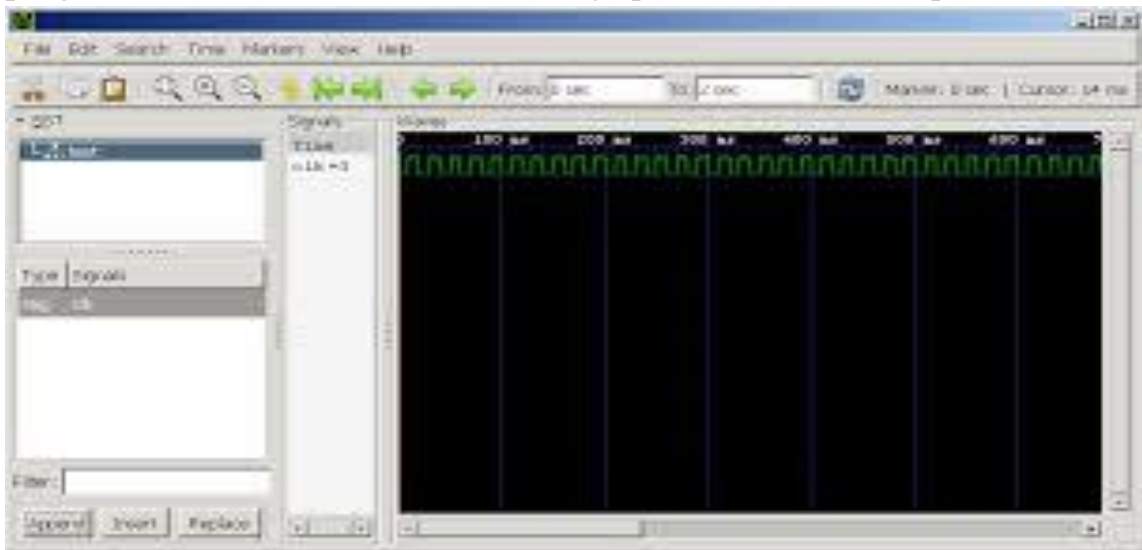
**Tema:** Quartus II programmasi signallarg'a islew beriw imkaniyatlarin paydalaniw.

Reje:

- I. Kirisiw
- II. Tiykarg'i bo'lim
  - a) Quartus II programmasi menen adimba adim tanisiw.
  - b) Quartus II programmasi menen signallardi qayta islew.
- III. Jwmaqlaw
- IV. A'debiyatlar

## Kirisiw

Quartus II a'meliy programmasi ha'zirgi zaman talabina say bolg'an talaplarg'a toliq juwap beriw imka'niyatina iye boldi. Endi biz Quartus II programmasi menen jaqinan tanisip shig'amiz.



1-suwret

Bunda kiriwshi signal 1-suwrette ko'rsetilgen. Og'an islew beriw protsessi to'mendegi izbe izlikte a'melge asiriladi.

Misal proekt simulyatsiyasin (Megawizard) megafunksiyasin eki sanin' qosiliwin ko'rip shig'amiz.

1. Proekt jaratamiz. Quartus II de.

2. Proektti bul faylidi Verilog Jodi menen jaratamiz, onin atin main ham og'an Top level entity di beremiz. Bul modul bas fayilda o'z ishine eki kiriwshi ha'm shig'iwshi boladi.

```
module main
```

```
(
```

```
input wire [7:0] in1,
```

```
input wire [7:0] in2,
```

```
output wire [15:0] out
```

```
);
```

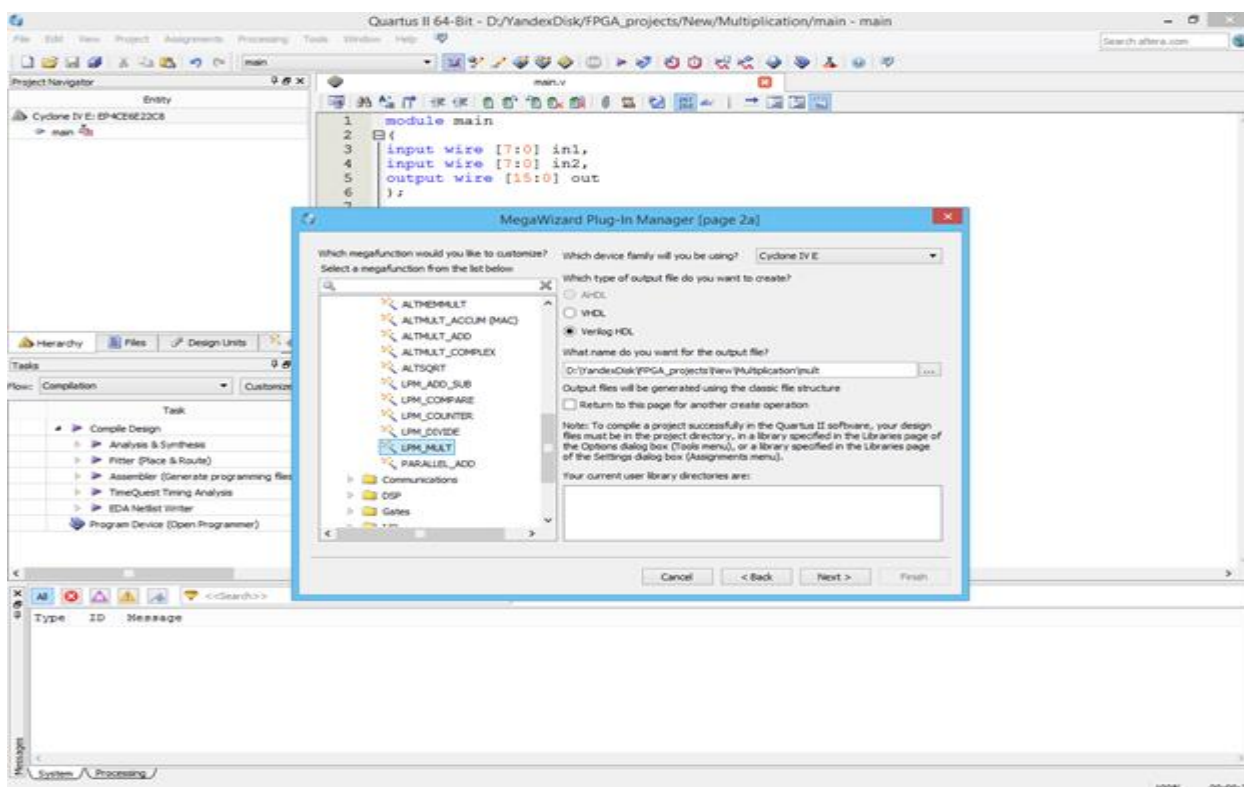
```
endmodule
```

3. Proektge megafunksiya (MegaWizard) ko'beytiwshi qosamiz. Bunin' ushin Tools->MegaWizard Plug-In Manager.

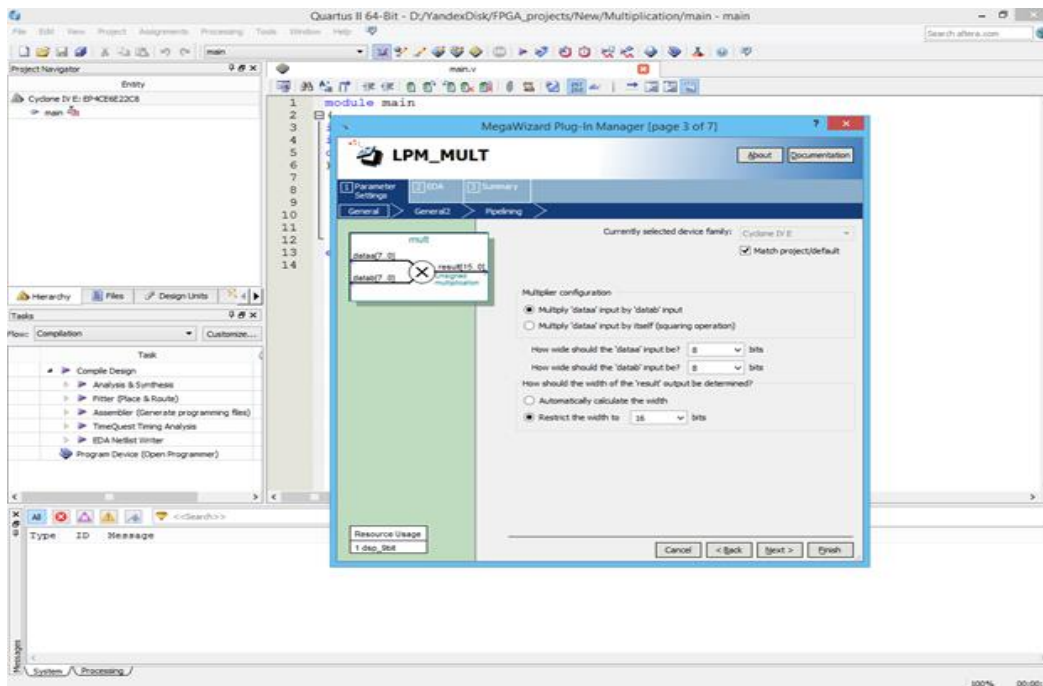
4. Dialog aynasinan Create a new custom megafunction variation saylaymiz.

5. Keyingi dialogda bizin' jan'a moduldin' atin beremiz, yag'niy MegaWizard aniqlanatug'in bul at boladi mult.

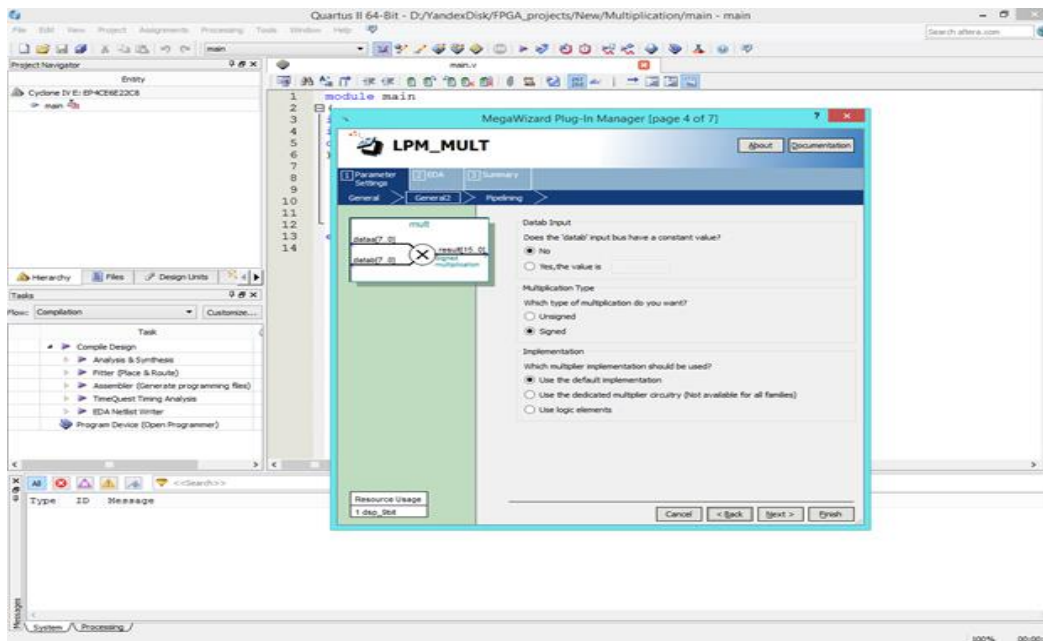
6. Bul dialogda terek siyaqli Installed Plug-Ins al onin' shaqasi Arithmetic onan keyin LPM\_MULT saylaymiz ha'm next knopkasin basamiz.



7. Nastroikani qoyamiz kiriw 8 bit al shig'iw 16.

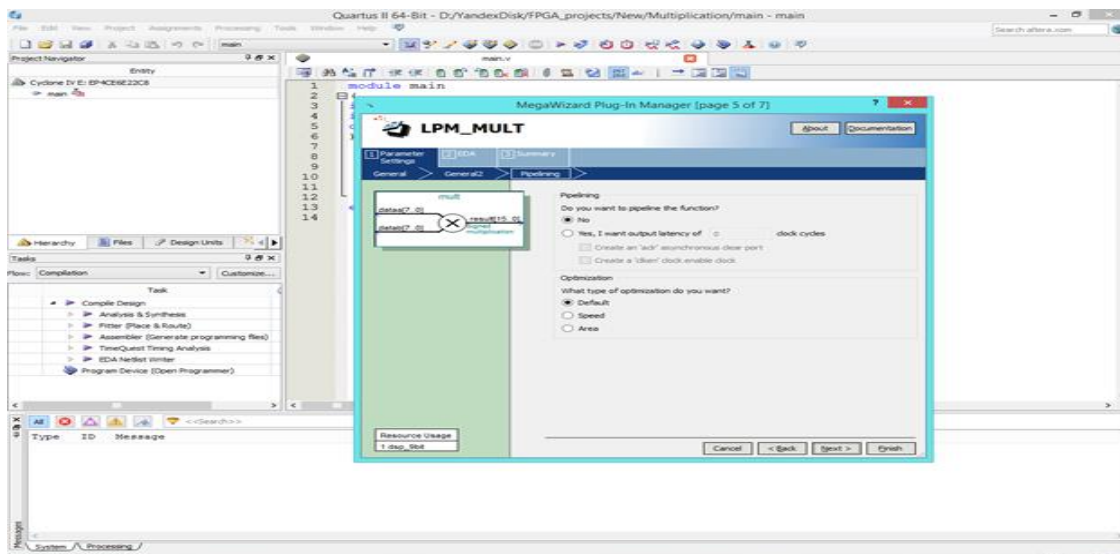


8. Keyingi dialogda nastroykni davam etiremiz: ekinshi kiriwshi ha'r dayim emes, ma'nislik ko'beytiwshi, realizatsiyani по умолчанию qollaw (kompilyator imkaniyatlarina qarap ishki jaylasqan ПЛИС ko'beytiwshilerin qollaniw, al olar jetpey qalg'an gezde ko'beytiwshini logikaliq bloklar ja'rdeminde realizatsiyalaw).



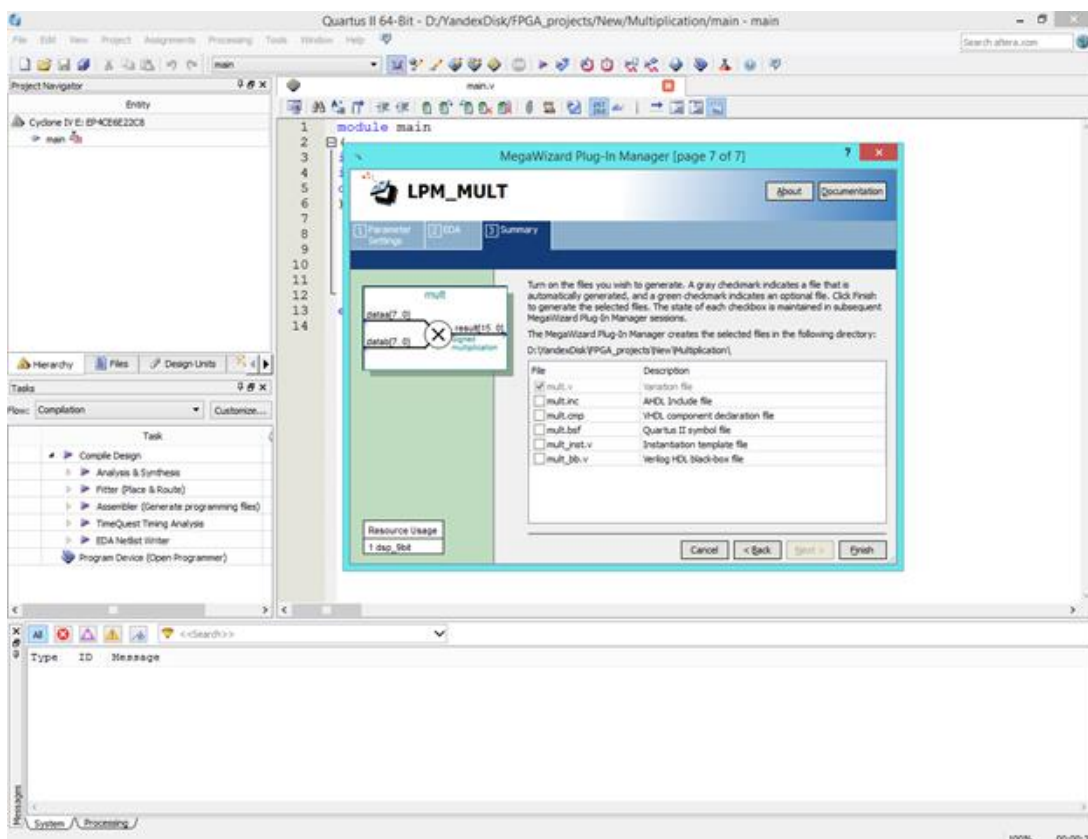
9. Keyingi dialogda realizatsiyalaw waqtinda конвейер(eger minani qollansaq , neshe taktli irkilis shig'iwshi signalda ) ha'm tip optimallasiriw korsetiledi. Конвейер di qollaniw ko'beytiwdi parallel operatsiyalar joli menen a'melge asiriw'g'a mu'mku'nshilik beredi. Yag'niy logikaliq bloklardi ekanomlawg'a (ishki

ornatlg'an ko'beytiwshiler joq jag'dayinda ), biraq ko'beytiw operatsiyasi bul jag'dayda ko'plew waqiti talap etedi.



10. Endigi dialog informatsiya xarakterin alip ju'redi, simulyatsiya waqtinda qanday kerakli bileotekalar kerak ekenin.

11. Endigi dialog qanday fayillar jaratilatug'unin jumis masteri aqirina qarap ko'rsetedi. Файл mult\_bb.v не нужен



12. Finish knopkasin basamiz ha'm usi proektke fayil qosilg'anin tasiyqlaymiz.

13.Sgeneratsiyalang'an fayildi Project Navigator fayl vkladkasinan tapsa boladi.

14. Oni aship mina kodti ko'riwge boladi.

```
// synopsys translate_off
`timescale 1 ps / 1 ps
// synopsys translate_on

module mult (
    dataa,
    datab,
    result);
    input  [7:0] dataa;
    input  [7:0] datab;
    output [15:0] result;
    wire [15:0] sub_wire0;
    wire [15:0] result = sub_wire0[15:0];
    lpm_mult  lpm_mult_component (
        .dataa (dataa),
        .datab (datab),
        .result (sub_wire0),
        .aclr (1'b0),
        .clken (1'b1),
        .clock (1'b0),
        .sum (1'b0));
```

```

defparam

    lpm_mult_component.lpm_hint = «MAXIMIZE_SPEED=5»,

    lpm_mult_component.lpm_representation = «SIGNED»,

    lpm_mult_component.lpm_type = «LPM_MULT»,

    lpm_mult_component.lpm_widtha = 8,

    lpm_mult_component.lpm_widthb = 8,

    lpm_mult_component.lpm_widthp = 16;

endmodule

```

Bunda kiriwshi ha'm shig'iwshi jaratilg'an moduldi ko'rse boladi mult – dataa, datab, result.

15. Megafunktsiyani qosamiz bas modul ko'beytiw main:

```

module main

(

input wire [7:0] in1,

input wire [7:0] in2,

output wire [15:0] out

);

mult mult01(.dataa(in1), .datab(in2), .result(out));

endmodule

```

16. Tuwrig'in tekseriw ushin kompilyatsiya qilamiz. Kompilyatsiyadag'i otchetta Ko'rsetilgen bir qosiliwshi ko'rsetilgen.

17. Proekt direktriyasina testbench TV\_main.v jaratamiz to'mendegishe ko'riniste.

```

`timescale 1 ms / 1 ns // o'lshe birligi waqit/ aniqliq model waqti(1, 10, 100)

```



```

module testbench_main;

reg [7:0] input_a;

reg [7:0] input_b;

wire [15:0] out_c; // shig'iw ushin

//testlenip atirg'an modul kopyasin ustanovka qilinadi main main1(input_a,
input_b, out_c);

// blok initial tek g'ana bir ret islenedi

initial

begin

input_a = 8'd255;

input_b = 8'd11;

end

// Tawsilip atirg'an simulyatsiya waqit momentinde 400 edenitsa waqit modelinde

initial

begin

#100000 $finish;

end

endmodule

```

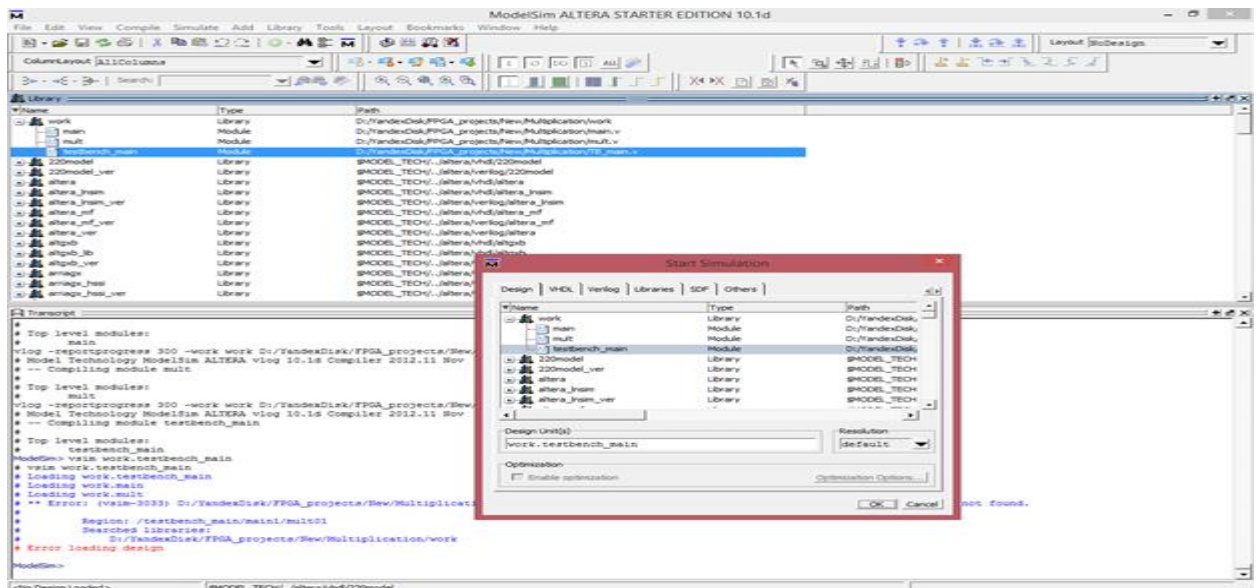
18. ModelSim di iske qosamiz ha'm direktoryasin o'zgeritemiz usi proekti (File->Change Directory)

19. A'melge asiramiz Compile->Compile ha'm main.v fayilin saylaymiz, TB\_main.v, mult.v, Compile knopkasin basip kompilyatsiya qa'tesiz juwmaqlang'anin ko'riwimizge boladi.

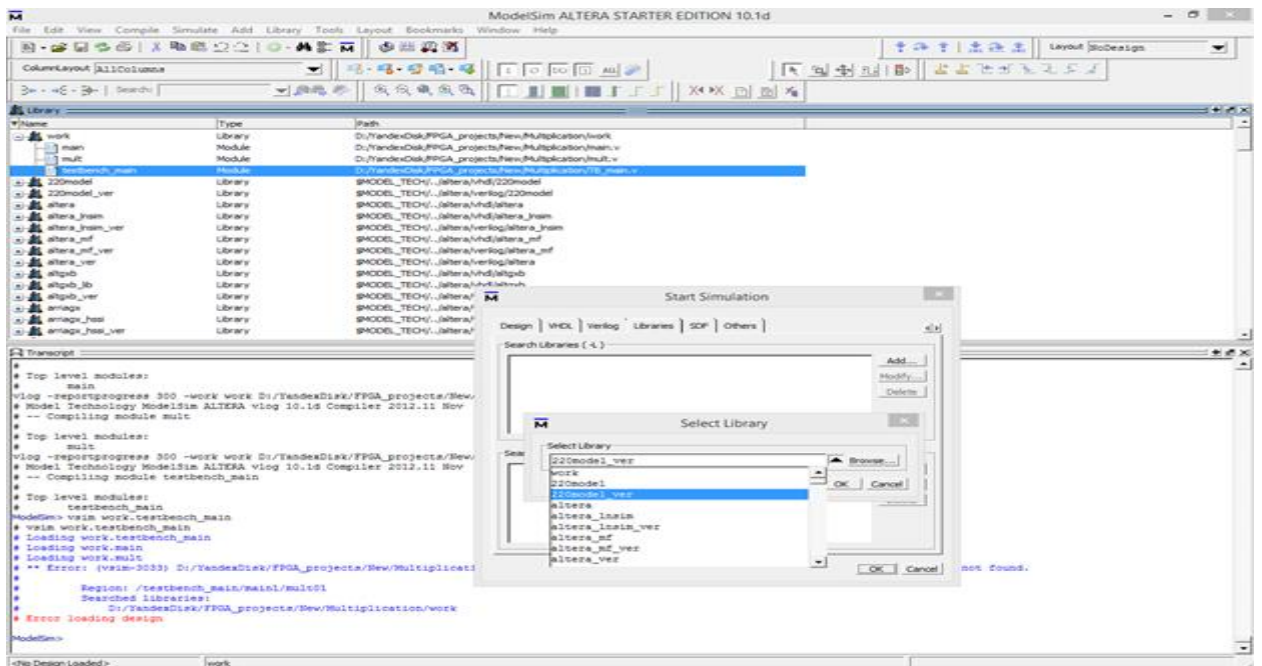
20. Simulyatsiyani iske qosamiz. Simulyatsiyani iske qosiw mishkanin' shep jag'in eki ret testbench(TB\_main.v)baslag'an qolayli. Biraq megafunktsiyanin' bibleotekalarin qollang'anda bibleotekag'a qosiliw za'ru'r,olardin' qatarina

kiriwshi ModelSim-Altera, ko'binese eki basiwdan TB\_main.v simulyatsiyani iske qosiwshi usi direktoryada izlew modul menen . Sonin' ushin simulyatsiyadan qollanilg'anda bibleotekaliq megafunksiyani qosiw Simulate->Start Simulation joli menen a'melge asiriladi.

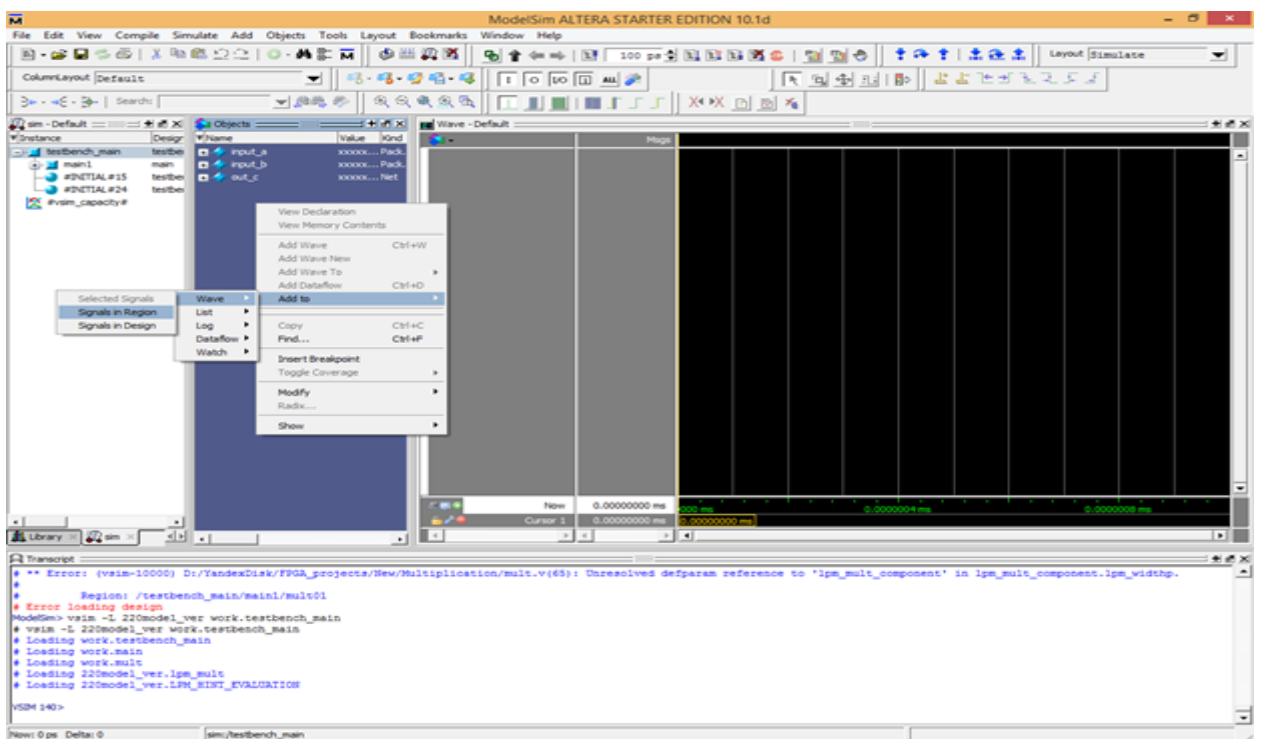
21. Ashilg'an dialogda testbench saylaymiz



22. Libraries vkladkasinda aynada search Libraries basiladi Add, ham aynadag'I strelkadan to'menge qatardan standartniy bibleotekadan библиотеку 220model\_ver(ol jerden lpm\_ver biraq 220model\_ver ko'pshilik funksiyalardi o'z ishine aladi , ha'm oni oylanbastan qosa boladi ). Ko'setilgen bibleoteka atlar ishinde ver-verilong ma'nisin bildiredi, bul yag'niy gilitli so'z, saylawda 220model qosilg'anda simulyatsiyasi qatelik payda boladi «Unresolved defparam reference to 'lpm\_mult\_component'». Bul qa'telik kanstanto parametri Verilongda ha'm VHLD o'z aldina ayrilip turadi.

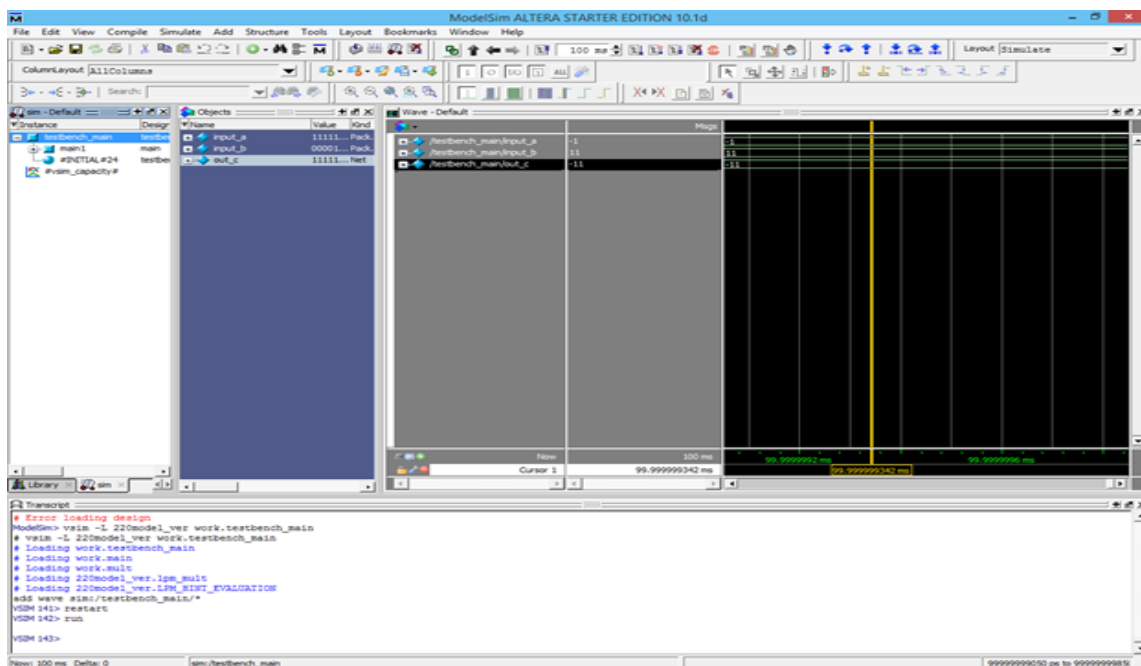


23. Ashilg'an aynada Objects kontekstli menyudi shaqirip Add to ->Wave -> Signal in Region a'melge asiradi.



24. F9 basamiz ha'm simulyatsiya na'tijesin tekseremiz.

25. Aynada Wave kontekstli menyudi shaqiramiz ha'r bir signaldi ha'm Radix bo'liminde Decimal di saylaymiz (Megafunktsiyani yaratqanimizda bizler ko'beytiwshi tip belgisin qollandiq).

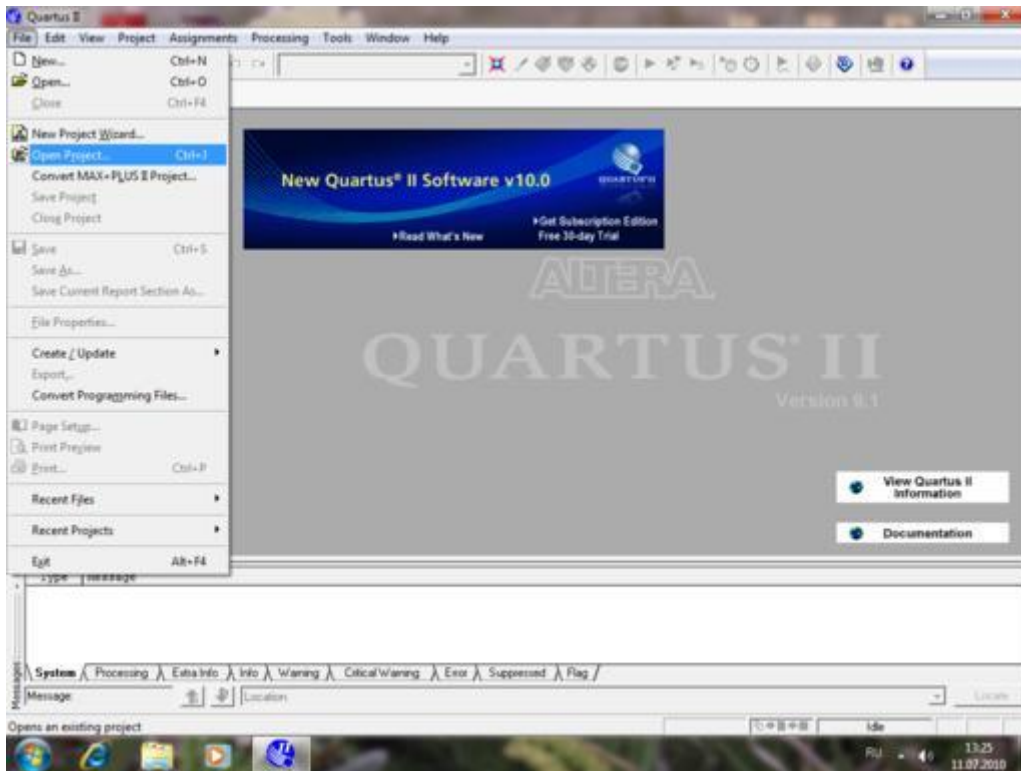


26. Simulyatsiya juwmaqlandi Simulate->End Simulation.

### Quartus II summator isleyviz.

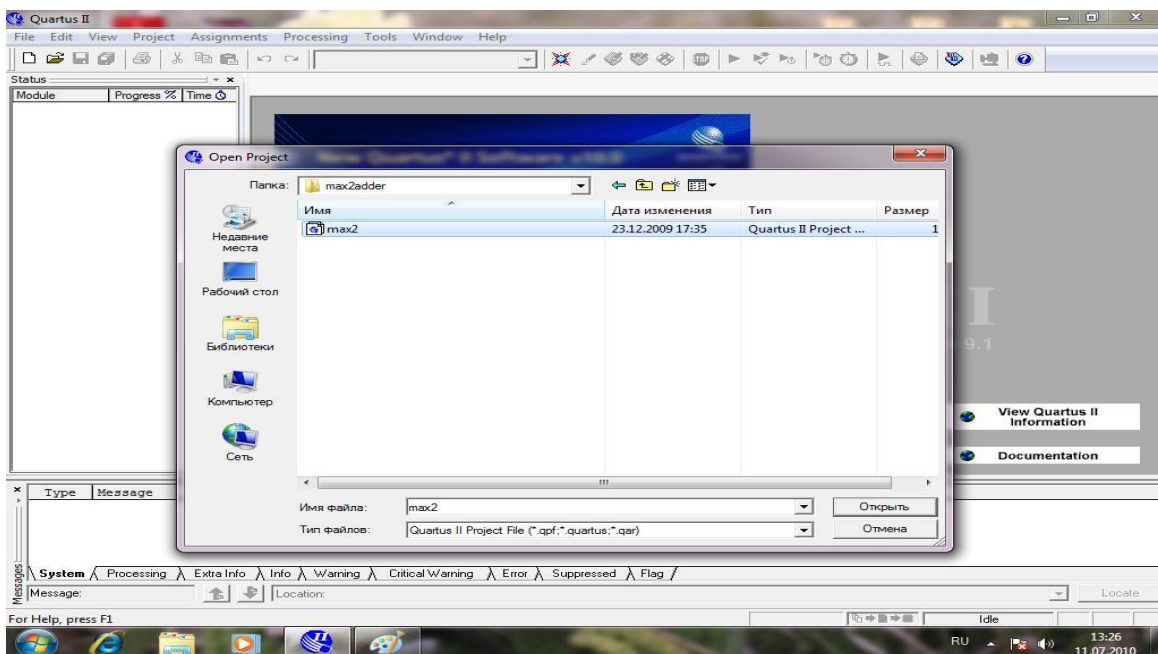
Kishi proekt Marsahod platasi ushin. Proekt bir neshe modullerden turadi, ha'm ol dim da u'lken jumisti atqarmaydi yag'niy eki bitli ni йщыщпэф imkan beredi. Bizin' platamizda 4 knopka bar. Ekewi – bir ekibitli san ha'm qalg'an eki knopka eki ekibitli san . Na'tiyjeni qosiliwshini Marsahod platasi svetadiodinda ko'rsetemiz. Biz Quartus programmaliq ortalig'inda sxema sizip u'yrenemiz.

Adim 1. Basta o'zimizdin' saytan pustoy proekt alamiz. Taza papka jaratamiz **max2adder** ati menen ha'm Quartuzdi iske qosamiz.



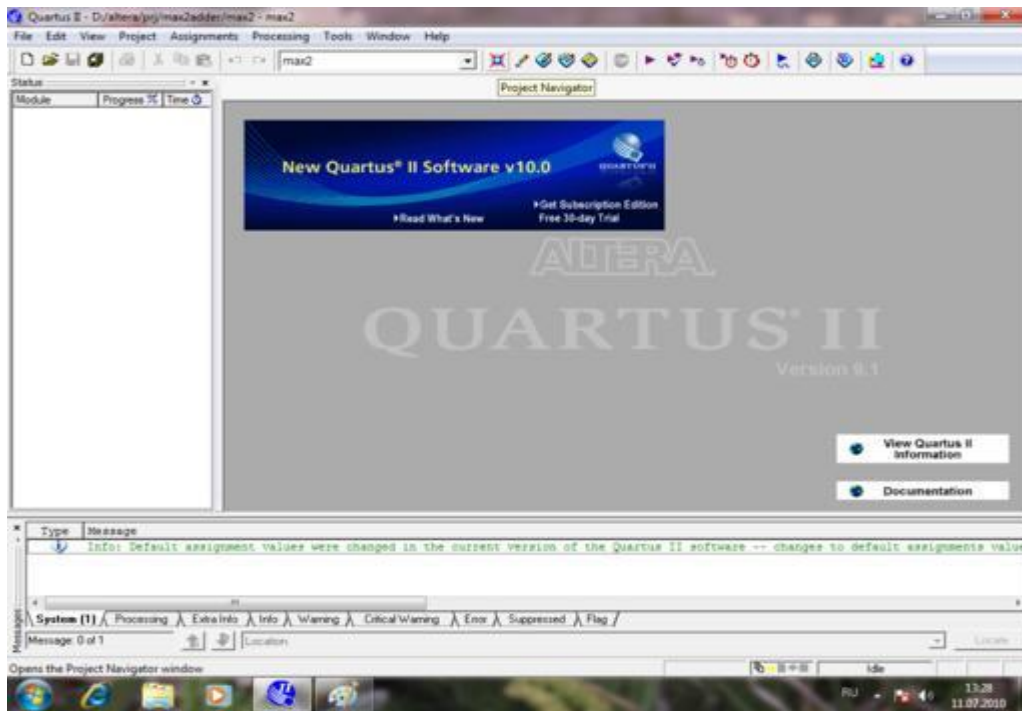
Menyu ge kirip Open Project punktini tan'lap oni ashimiz.

Adim 2.



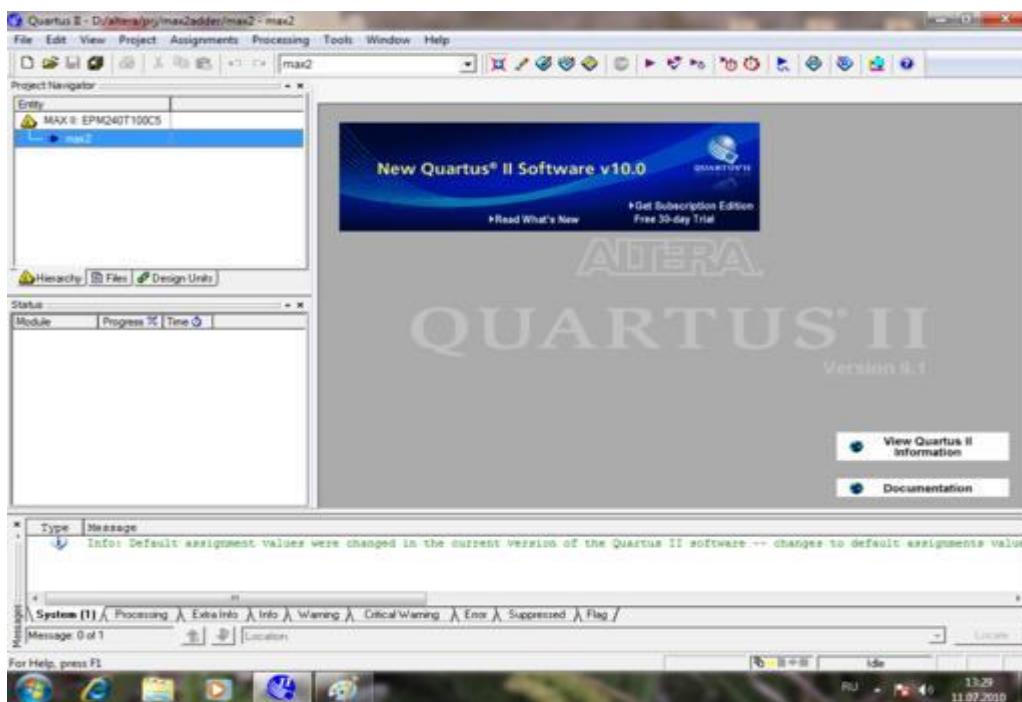
Fayildi tan'law ushin dialog aynasi ashiladi . Onan biz bizin' yaratilg'an papkamizg'a **max2adder** kirip ha'm Proekt max2 faylin saylaymiz.

### Adim 3.



Proekt ashiq biraq esh narse visualno qilinbadi. Proekt ati endi biz yaratqan taza proekt penen ataldi. Tishqanshani panel istrumentke alip kelemiz , kristaldi esletiwshi. Ha'm oljerde pod skazka payda boladi "Project navigator" usi knopkani basamiz.

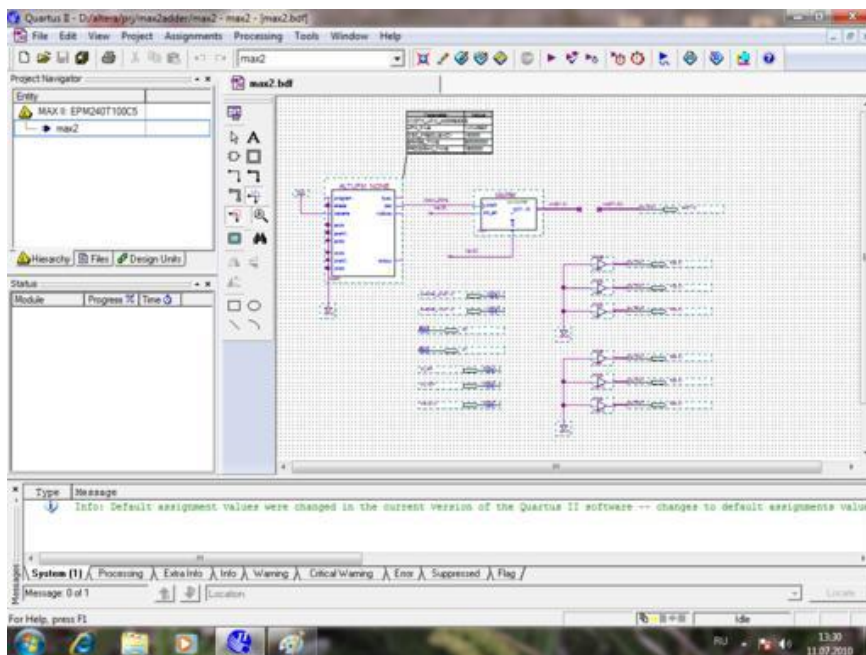
### Adim 4.





Shep tarapte proekt navigator aynasi payda boldi. Onin' u'sh zakladkasinda proket ierarxiyasini ko'rsatib beriladi (qaysi bas modul ha'm quramindag'i) ha'm onan basqa proekt fayillari. Tishqansha eki ret basamiz bas modulge max2 ha'm fayl ashiladi, bas modul haqqida toliq mag'lumat (**top-level entity**) ta ko'rsatilgan.

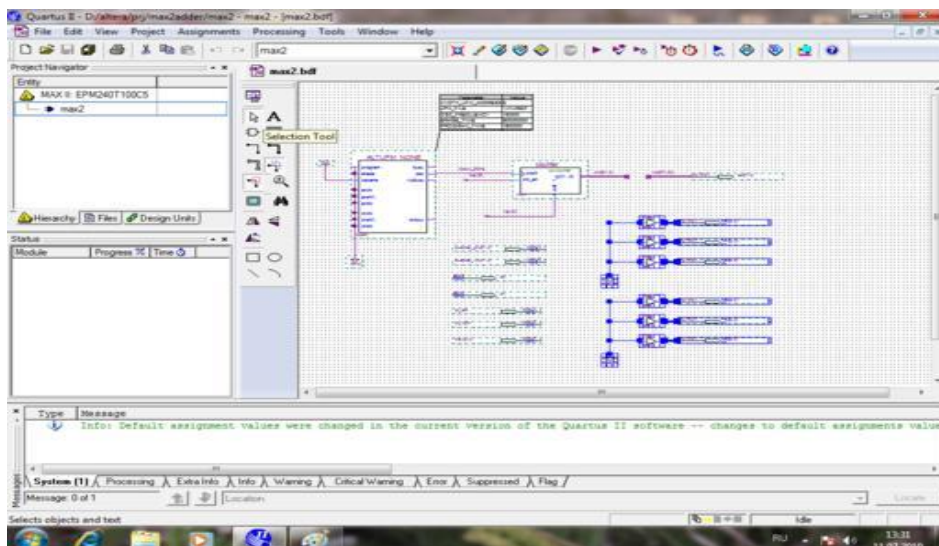
Adim 5.



Max2.bdf grafikaliq fayili ashilg'anin ko'remiz **max2.bdf** – bul Block Diagram File.

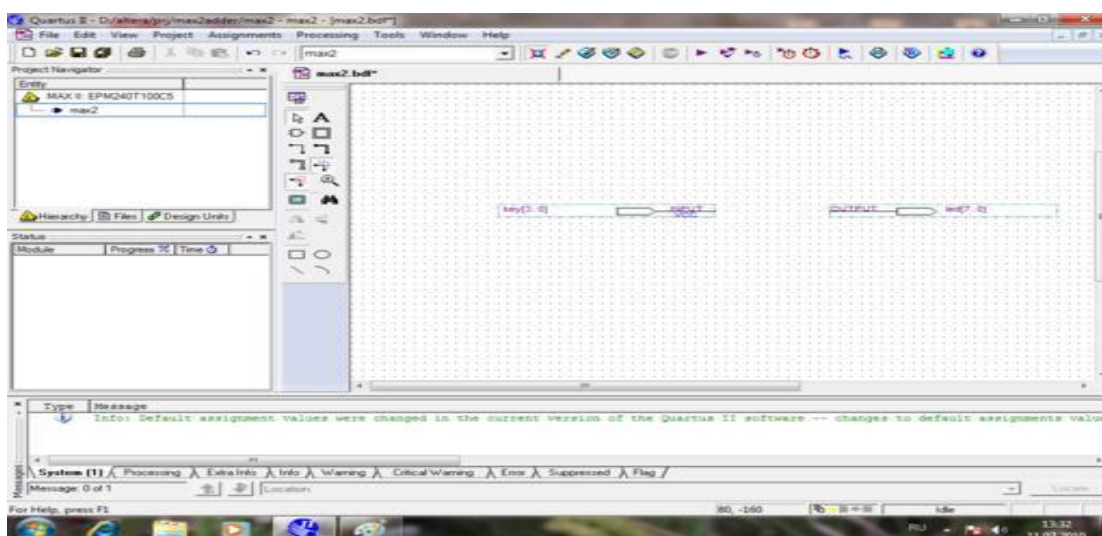
A'llette proekt bas fayili grafikaliq tu'rde bolivi kerek emes. Bul Verilog yaki VHDL yaki onan basqasi da bolivi mu'mku'n.

Adim 6.



Xa'zir biz bul shala pustoy proekten tap taza proekt qilamiz. Panel instrumenti basamiz knopkasin strelka tarizli suwreti menen - Selection Tool- obiyektlerdi belgilep aliw instrumenti. Bizin' sxemamizg'a basip olardi belgilep aliwmiz mu'mku'n olar belgilengende aspen ko'k ren'ge kiredi. Klaviaturadan **Del** knopkasin basamiz ha'm belgilengen obiyekt yaki grupppa o'shiriledi. Men bul proektte tek g'ana to'rt kiriwshi **key[3..0]** (olar Marsaxod platasindag' knopkalg'a tuwra keledi) ha'm shig'iwshi **led[7..0]** (olar segiz svetadiodg'a tuwra keledi).

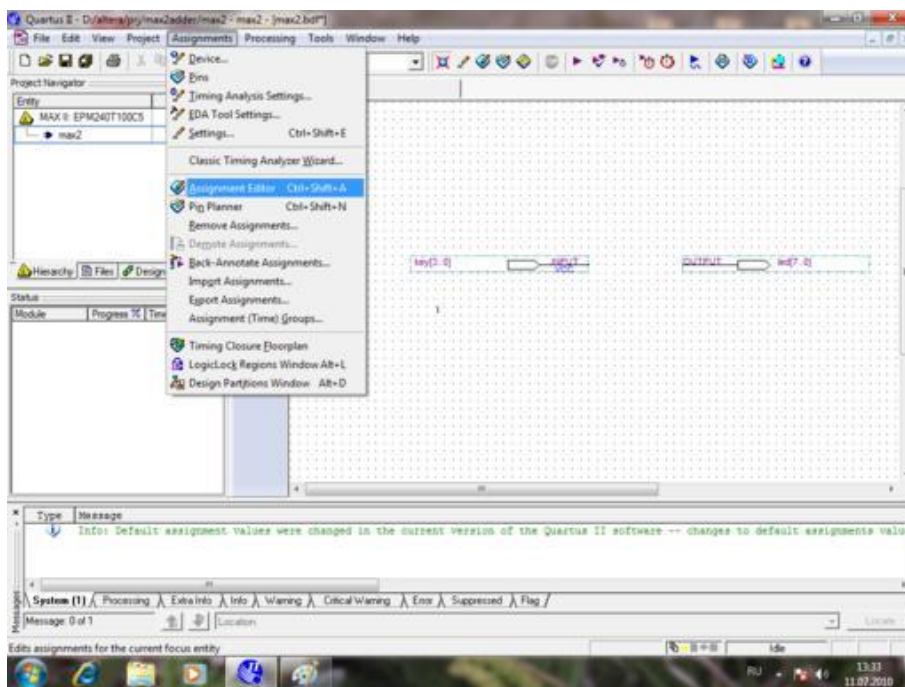
Adim 7.



Mine mende boar sxemadan ne kalg'anin ko'riwin'izge boladi. Buni nege islep atiripan taza proektten baslag'an jaqsilaw boladi, yaq negeki bul proektte en' kerekli nastroykalar ornatilg'an Marsaxod platasi ushin sonin' ushin da taza proekt alip oni tazaladiq. Bul nastroykalar mikrosxema tiplerine baylanisli ha'm kontakt mikrosxemasi bo'listiriliwin aytsaq boladi. Buni an'sat teksersek boladi.

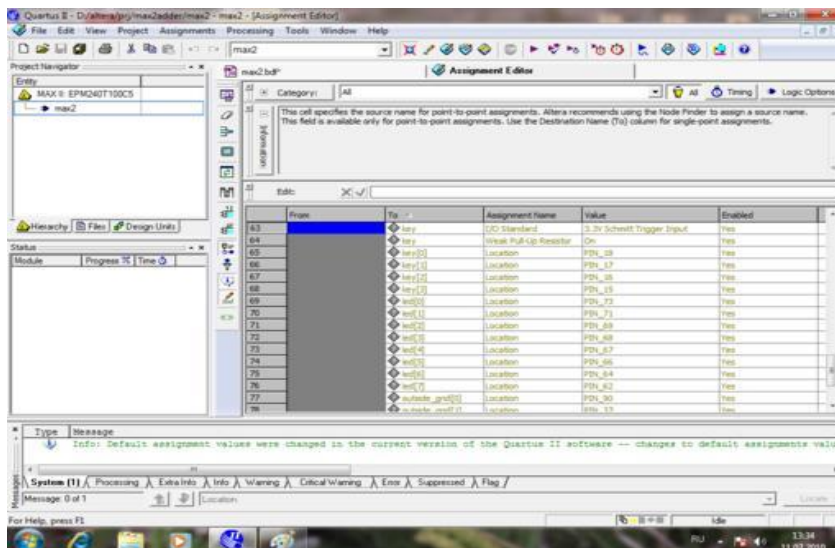


## Adim 8.



Assignments\Assignment Editor ge kiremiz (redactor naznachanyasin iske tu'siredi).

## Adim 9.

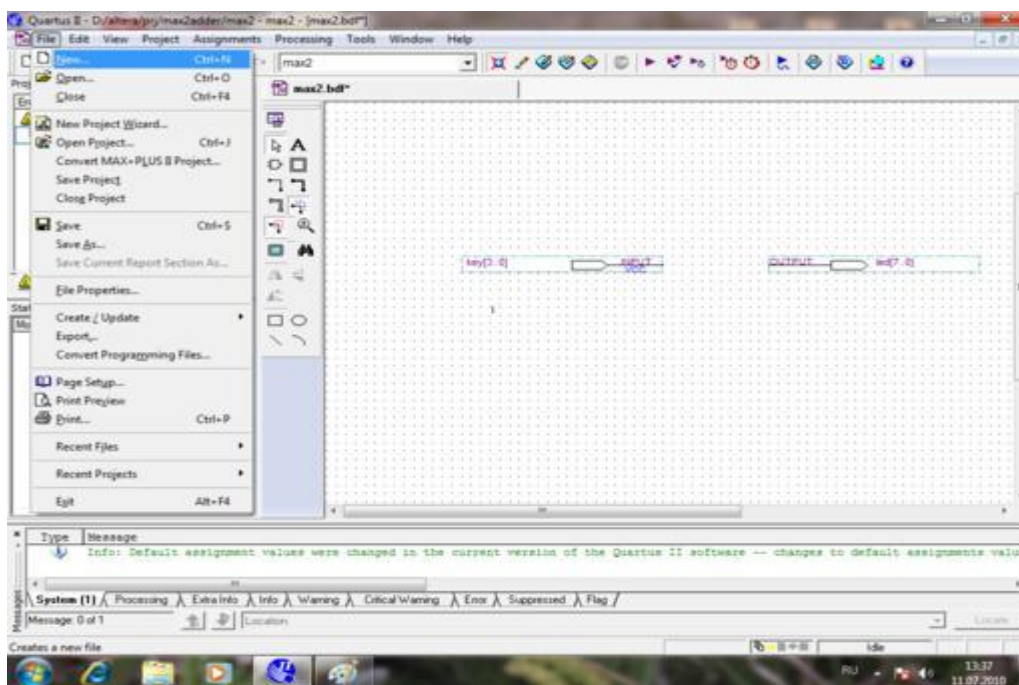


Misalan bul jerde ko'rinit turipti mas keliwshi kiriwshi Marsaxod platasinag'i knopkag'a mikrosxema kontaktlerindegi PIN\_18, PIN\_17, PIN\_16, PIN\_15 jalg'anadi. Tap usinday basqa joli boliwi da mu'mku'n emes. Plata uje tayin boldi paykilendi ha'm bul kontaktler knopkalg'a baradi eger siz o'zin'izdin' ustroystvan'izdi [FPGA](#) yaki CPLD da qilmaqshi bolsan'iz kiriwshi shig'iwshi

knopkalarin'izdi o'zin'iz bersen'is boladi. Onda Marsaxod Platasi menen eksperiment otkeremiz. Oni barlig'insh qabil etemiz.

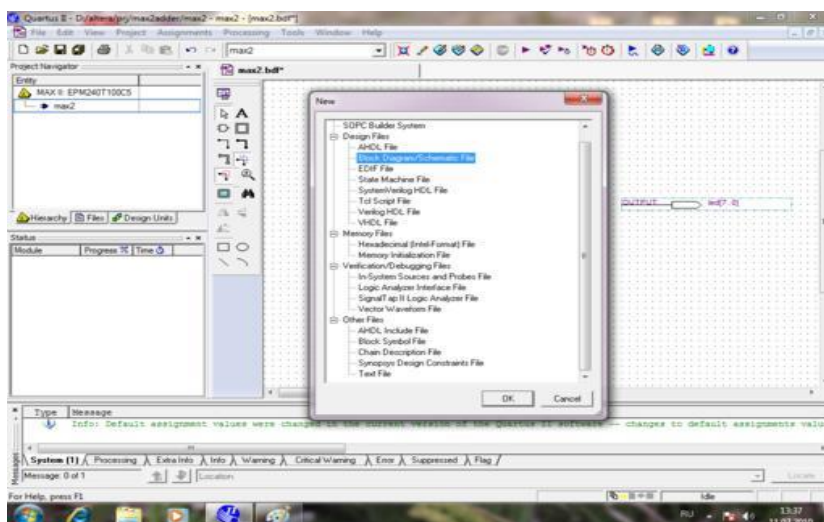
Redaktoe naznachenieni jawamiz.

Adim 10.



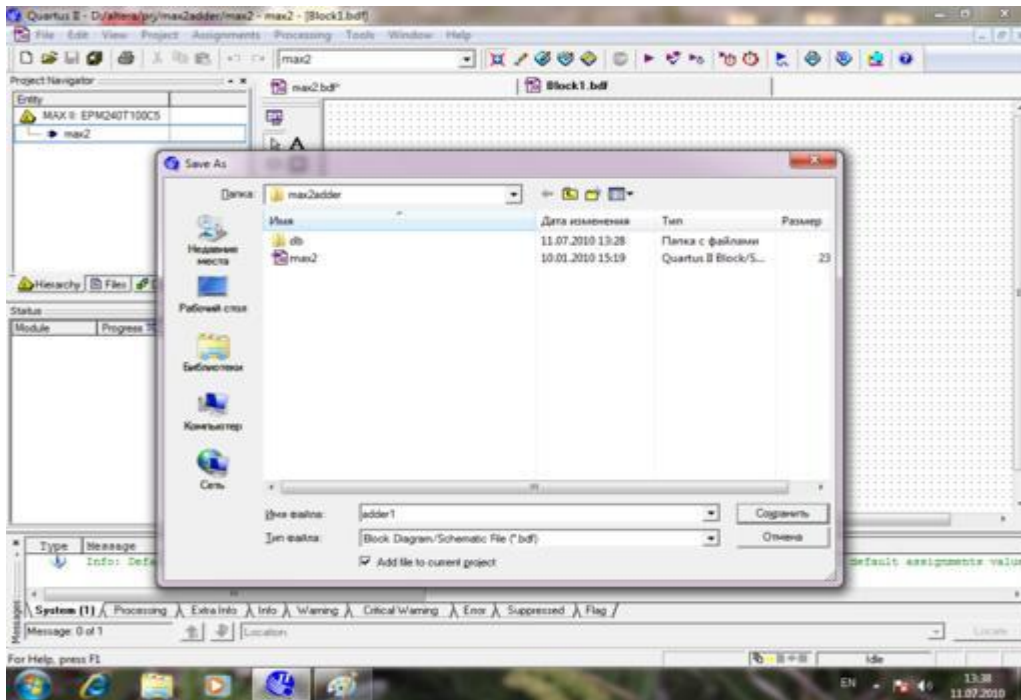
Endi jan'a fayil jaratamiz. Menuden **File/New** saylaymiz.

Adim 11.



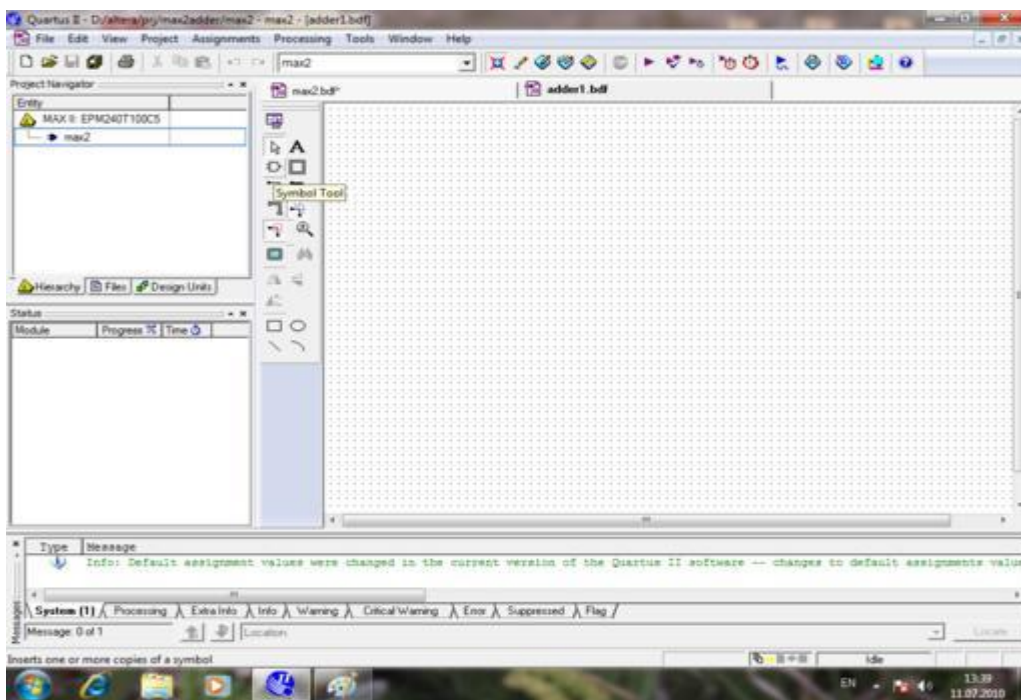
Bul dialogda fayildin' tipin saylaw imkaniyati bar, jaratiliwshi fayildin'. Xa'zir **Block Diagram/Schematic File** saylaymiz ha'm sxemani siza baslaymiz.

Adim 12.



Jan'a grafikaliq fayil yaratildi ha'm oni satronit eiwimiz kerek-men bug'an **adder1.bdf** atin beremen.

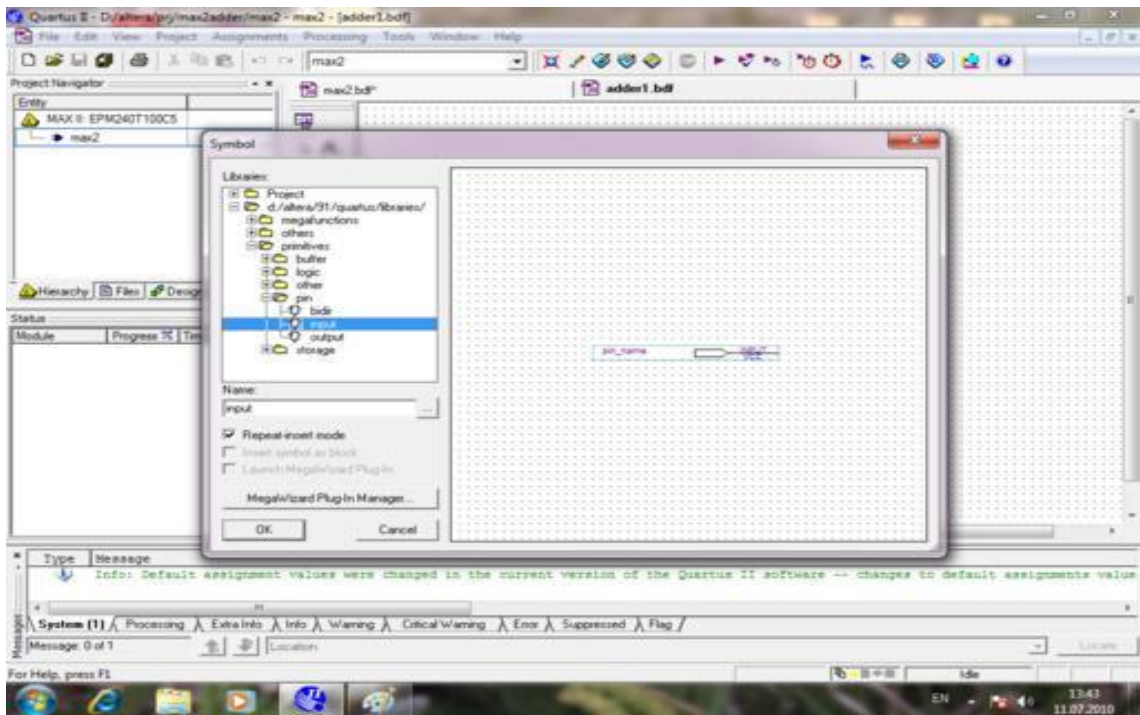
Adim 13.



Panel instrumentinde knopkani suvret pene logikaliq element korip tursizba (podskazka "**Symbol Tool**").

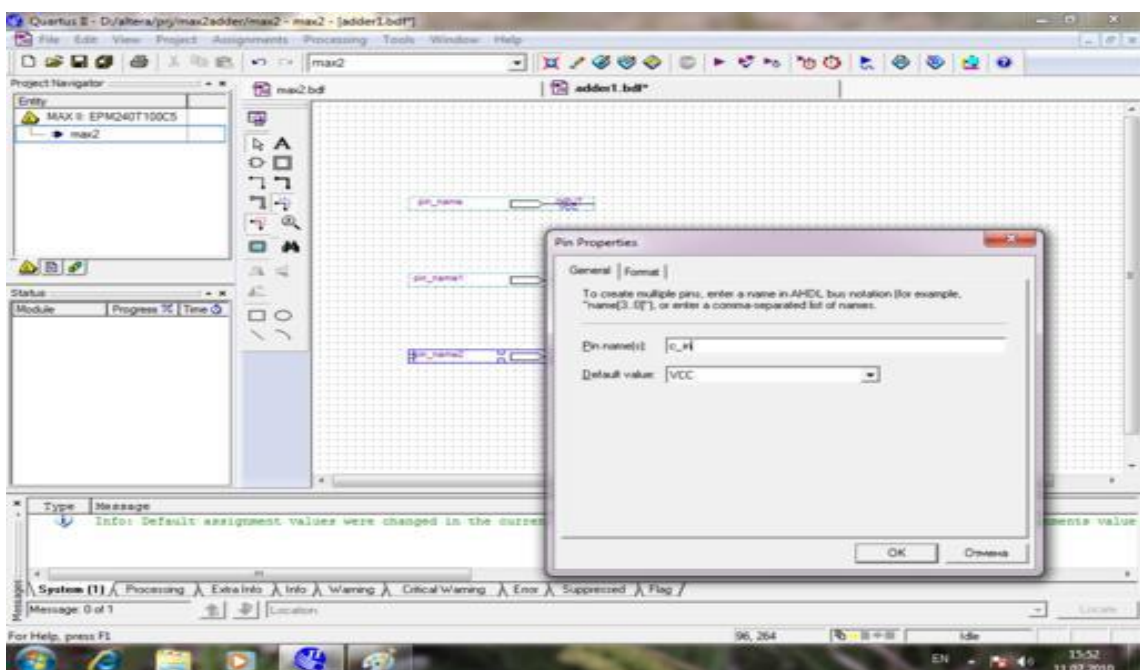
Knopkani basqanimizdan keyin dialog aymasi shig'iw kerek, bizge kerekli logikaliq element bibleotekasin saylawg'a ja'rdem beriwshi.

#### Adim 14.



Bul **Symbol** dialogi. Bizin' sxemamiz kiriwshi ha'm shig'iwshi boladi ha'm bir neshe logikaliq logikaliq elementen. Bibleoteka papkalari arasinan (**libraries**) tabiw kerek **primitives/pin/input**. Ha'm ok basamiz biz ta'repten belgilengen element sxemada payda boladi.

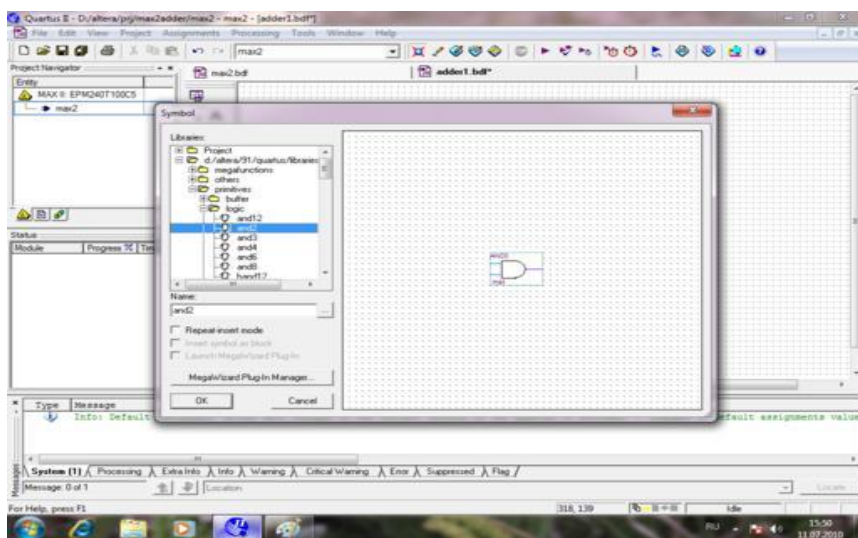
#### Adim 15.





Bizlarga sxemag'a u'sh kiritishni ornatishimiz kerak. Bul grafikaliq redaktor ju'da qolayli. Siz ornatilga'an elementlarni an'sat qozg'atishimiz mu'mkin, buffer obyekti uchun kopya qilishimiz boladi, vstavit etsen'izde boladi. Kiritishlarga at bersek (ha'm onan basqa elementlarga) tishqanshanin' on' ta'repin basib belgilengen obyekti punk menuden Properties(свойства).Xazir kak raz siz ko'rip turg'anin'iz suvret kiritishni atlari o'zgartilgen (**pin**) dialoginde **Pin Properties**.

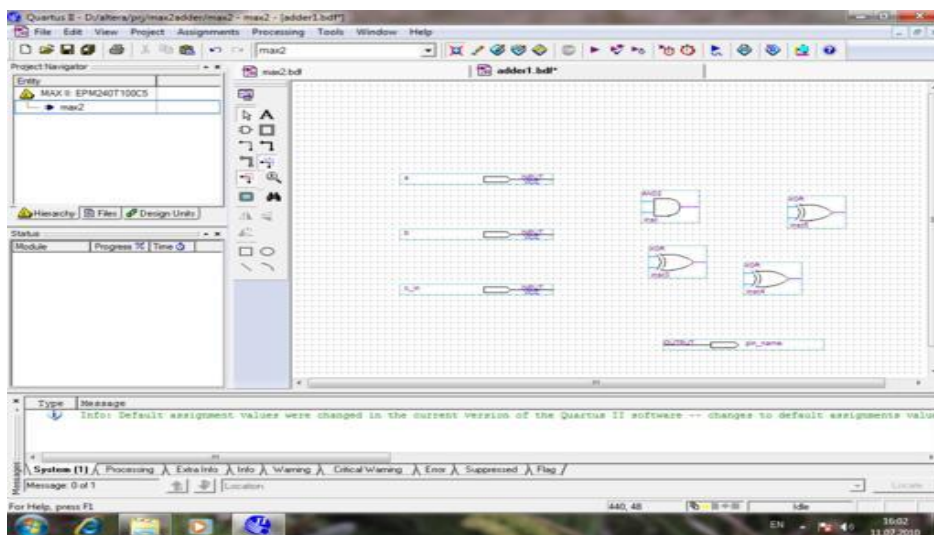
Adim 16.



Analogochnim obrazom sxemag'a shig'iwishi logikaliq element qoyamiz **И ha'm ИСКЛЮЧАЮЩЕЕ ИЛИ**.

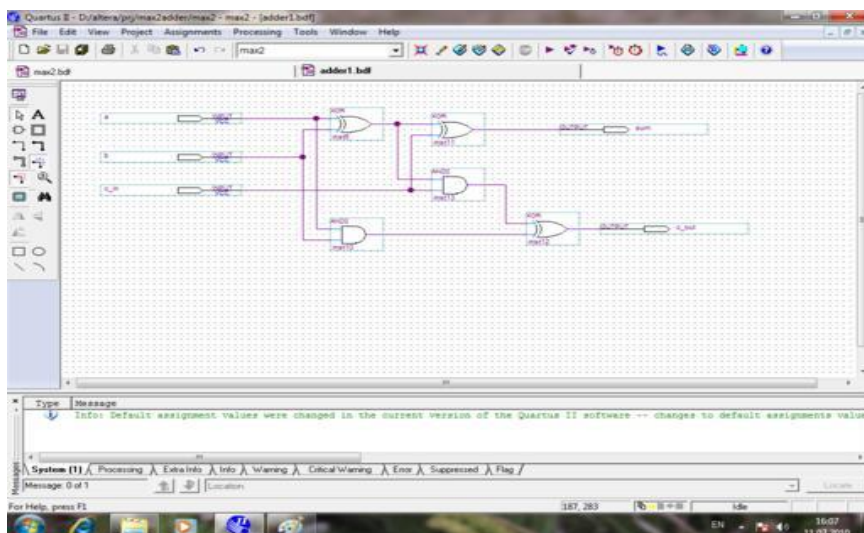
Oni **libraries/primitives/logic** papkasidan izlen'.

Adim 17.



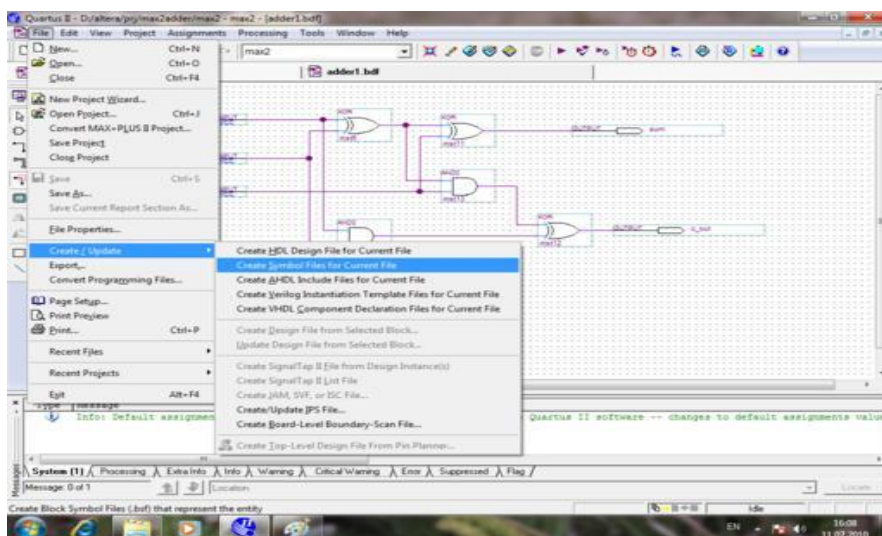
Endi bul elementlerdi sxemag'a slu qilip qoyip ha'm simlarg'a jalg'aw kerek. Simlar menen jalg'aw ushin panel instrumentten **Orthogonal Node Tool** tabin'. Keyin simdi prosti sizin'. Eger kerek bolsa shinani sizin', onda **Orthogonal Bus Tool** qollanin'.

Adim 18.



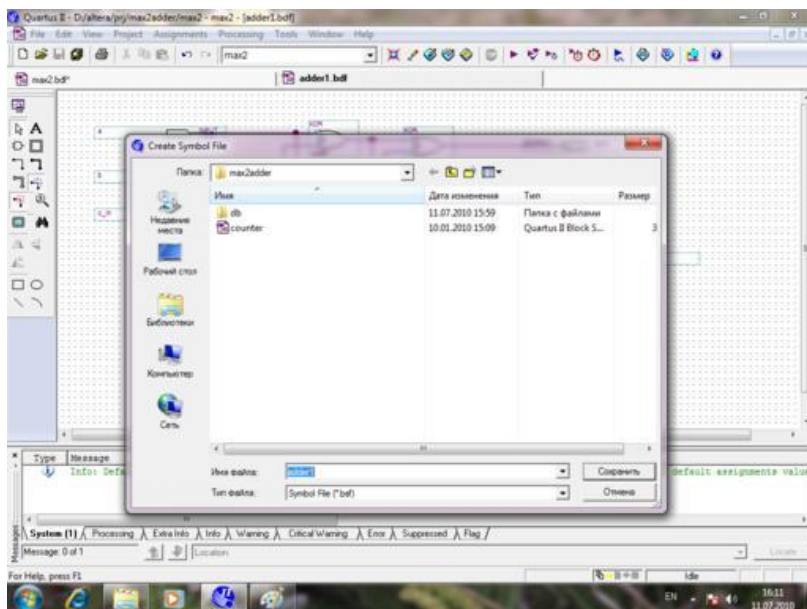
Mende minanday sxema payda boldi- bul qolayli summator daje alip ju'rsede boladi. Toliq mag'luwmat <http://marsahod.org> ko'rsetilgen. Endi bul modulden sxema ko'rinisindegi component isleselek boladi, ja'nede basqa modullerge ornatiw ushin.

Adim 19.



Punkt menudan **File/Create-Update/Create Symbol File for Current File** saylan'. Bul jan'a component yaratadi, yag'niy sizin' basqa sxemalarin'izg'a da ornatiw ushin. Verilog, VHDL, AHDL, fayilinan komponent sxemasin jaratsa boladi.

Adim 20.

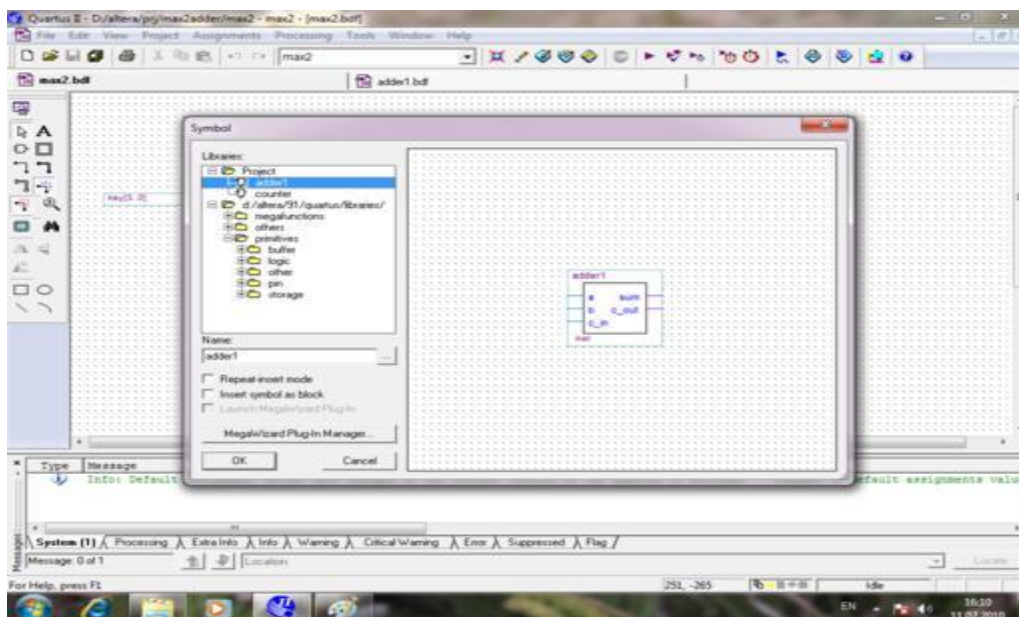


Itibar qaratin' xa'zir bizge jaratiliwshi kompananta atin jaziwimiz kerek.

По умолчанию ol schema ati menen duris keledi. Solay saxronit etip qoyayiq.

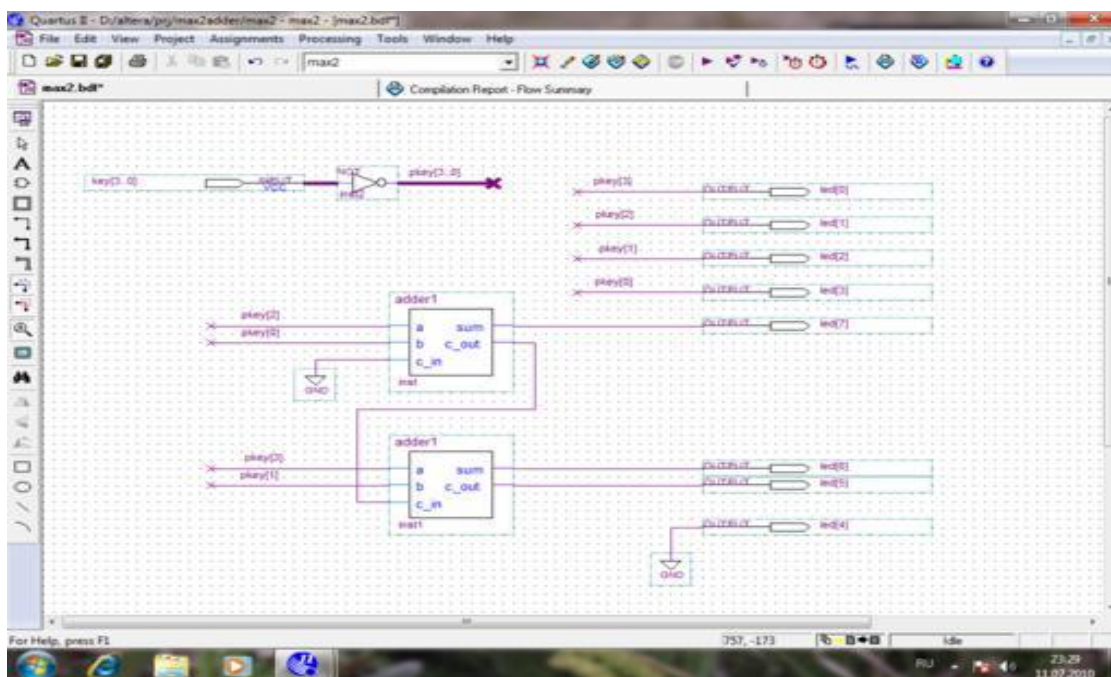
Fayildin' tipi - **Symbol File (\*.bsf)**.

Adim 21.



Endi biz bizin' birinshi faylilimiz **max2.bdf** redaktirovanie sina qaytayiq. Endi usi jerge bizin' jaratilg'an jan'a komponenta **adder1** di jaylastirsaq boladi. Panel instrument knopkasin basamiz **Symbol Tool** ha'm bizge jaqsi tanis dialog ko'remiz **Symbol**. Endi bunda komponentani alltera bibleotekasinan izlemeymiz al bizin' proekt papkasinan jan'a jaratilg'an komponenta ni alamiz.

Adim 22.



Biz bizin' sxemag'a eki komponenta **adder1** bir invertor **HE**, birneshe element **GND** (qolanilmay atirg'an kiriwshilerdi zemlyag'a jalg'aw ushin). Ha'mme elementlerdi suwreteri dey qilip jalg'an'.

Bilay jalg'ang'an birinshiden knopkasin basqan gezde og'an tiyisli svetadiod jansin(to'rt shep svetadiod ), ekinshiden ekibitli qosiliwshi na'tijesi u'sh on' svetadiodda ko'rinsin.

Soraw payda bolawi mu'mku'n nege signal knopkadan инвертируется?. Negeki signal knopkag'a jalg'ang'an onsha u'lken emes elektr energiyasina jalg'ang'an rezistorlar. Bul chip ishinde islengen **Assignment Editor** nastroykasinan ko'rse boladi **key[3.0]** knopkasi ushin. **weak pull-up resistor** opsiydi ko'resiz qosilg'an



(On). Solay etip knopkani baspay aq kiriste logikaliq edinitsa berdi, a basilsa logikaliq nol (замыкается к земле). Proekt tayin Kompilyatsiya isleymiz ha'm oni **Марсоход** Platasina jayg'astiramiz. Plitag'a qalay biriktiriv tuwrali mina jerde ko'rsek boladi <https://marsahod.org/11-blog/> .

Bizin' platani a'melde sinawdan aldin ekilik qosiw misalin sizge ko'rsetsem.

$00 + 00 = 000$  (nol + nol = nol)

$01 + 00 = 001$  (bir + nol = bir)

$01 + 01 = 010$  (bir + bir = eki)

$10 + 01 = 011$  (eki + bir = u'sh)

$10 + 10 = 100$  (eki + eki = to'rt)

$11 + 01 = 100$  (u'sh + bir = to'rt)

$11 + 11 = 110$  (u'sh + u'sh = alti)

Biz ko'riwimiz kerek bolg'an zat **Марсоход** platasindag'li knopkani basqanimizda.

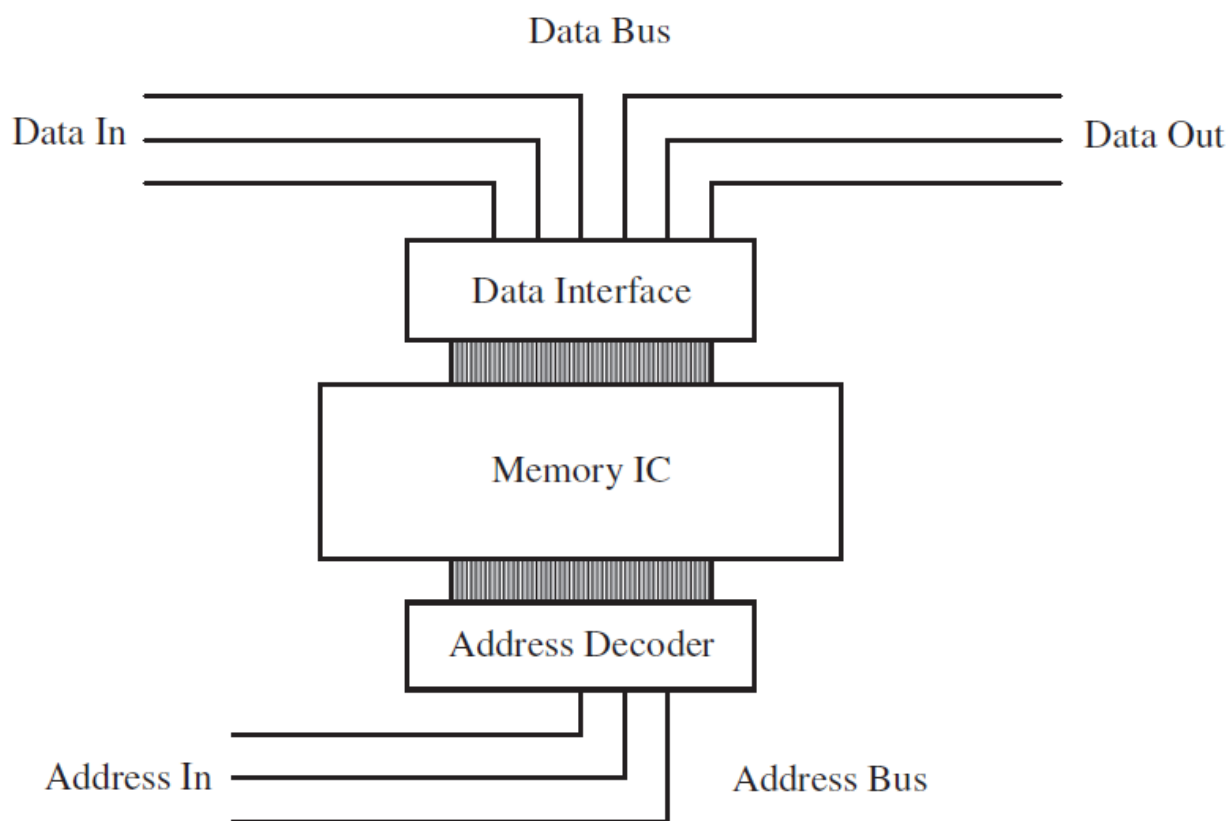
Mina jerde sabaqa tiyisli barliq proektler: [Двухбитный сумматор - к уроку Quartus II \(72.14 Кбайт\)](#)

*Bular ha'r dayimg'i yad, tez yad ha'm 1-darejeli KESH yadlar. Usi temalarda a'dette interfeys sirtta jaylasqan yamasa eki yad ha'm interfeys ishinde jaylasqan ha'm interfeys sirtta jalasqan yad haqqinda so'z baradi. Bulardan tisqari ROM 2-da'rejeli KESH ha'm tez yad siyaqli birlmshi yadlaar ha'm plitag'a baylaniaqan, biraq tuwridan tuwri interfeysge baylanispaytug'in eklemshi/u'shlemshi yadlar.(maselen: CD-ROM, jumsaq disk, qatti disk ha'm lentalar) haqqindag'I mag'liwmatlardi o'z ishine aladi. Birlmshi yad a'dette yad sistema bir bo'lek esaplananip, u'sh komponentlerden payda etiledi.(su'wret 3.3de ko'rsetilgen):*

*- yad mikrosxemasi;*

-adress shinasi;

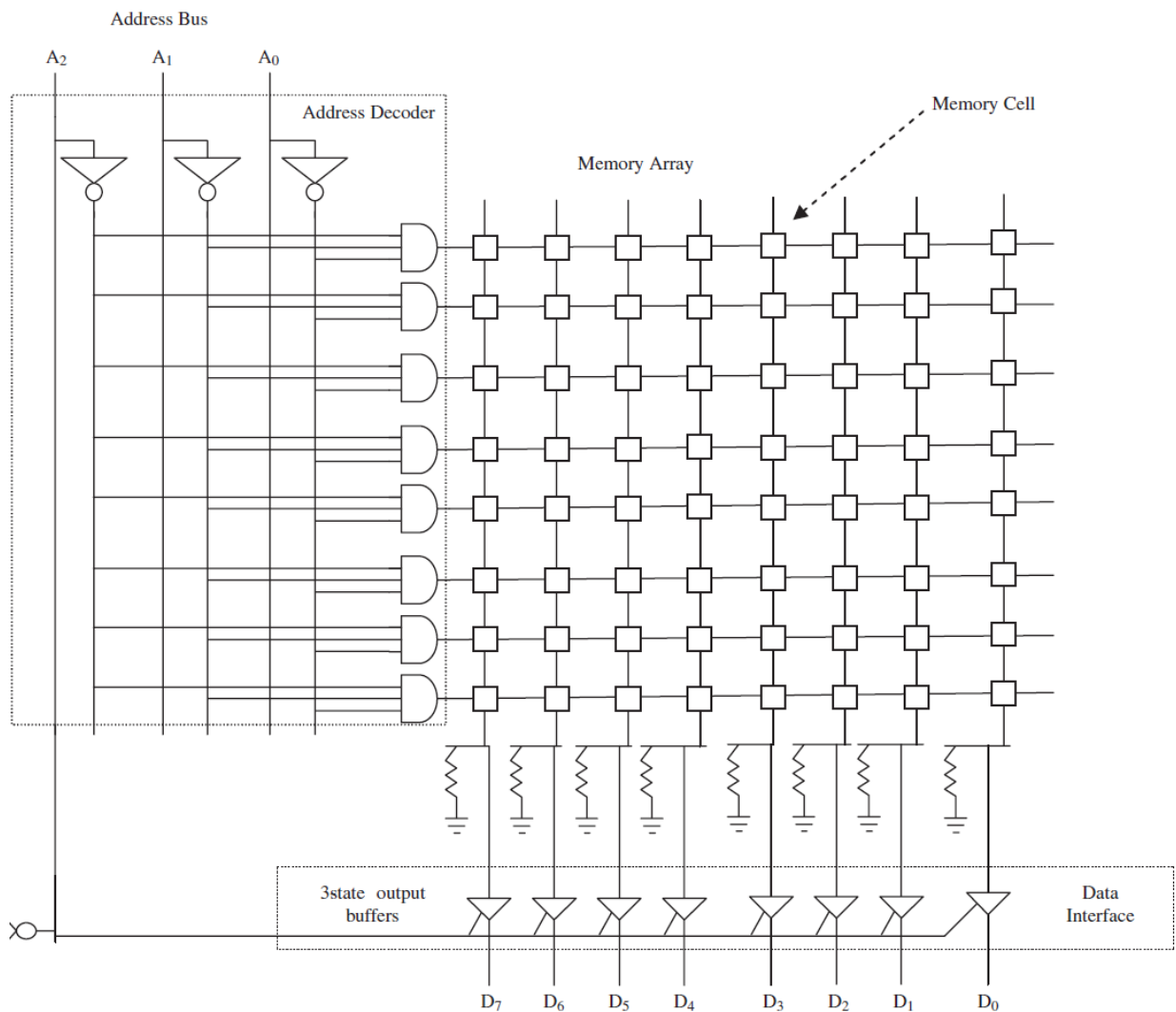
- mag'liwmat shinasi.



*Su'wet 3.3 Birlamshi yad sistema astindag'i apparat qurilma.*

*Uliwma alg'anda, yad integral sxemasi u'sh bo'limnen payda etilgen: yad massivi, a'dress deshipratori ha'm mag'liwmat interfeysi. Yad massivi tiykrinda mag'liwmat bitlerin saqlawshi fizikaliq yad. Interfeys ha'm programist yadqa bir o'lshemli massiv sipatinda mu'ra'ja't etilgende , ha'r bir massiv yasheykasi baytlar qatarin payda etedi ha'm qatardag'ilardi bitler sani o'zgeriwi mu'mkin. Negizinde ha'r bir yasheyka bir bit mag'lumatta saqlay alatug'in jalg'iz qatar ha'm bag'analarg'a iye adresslengen yad yasheykalardan payda bolg'an eki o'lshemli fizikaliq yad bolip tabiladi.*

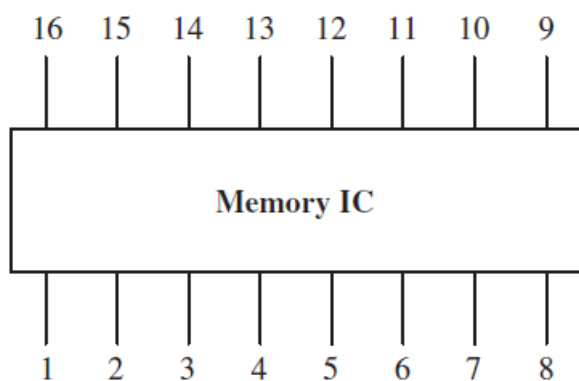
*Yad eki o'lshemli massiv ishinde ha'r bir elementler jaylasiwshi a'dette , bag'ana ha'm qatarlar parametrlerden payda bolivi yad fizikaliq adress dep ataladi.*



### Su'wret 3.4 ROM yad massivi

Integral sxemanin' qalg'an tiykarg'i komponenti adres deshipratori adres shina mag'liwmatlarga tayang'an halda yad massvine mag'liwmatlar adressin tabadi, mag'liwmatlar interfeysi bolsa mag'liwmatlardi uzatiw ushin mag'liwmatlar shinasin mag'liwmatlar menen ta'minleydi. Mag'liwmatlar ah'm adressler shinasi integral mikrosxema yad adressi deshiferlang'an ha;m mag'liwmatlar interfeysinen mag'liwmat aladi ha'm uzatadi. Yad tu'rine qarap, plitag'a baylanisiwshi my'mkin bolg'an yad mikrosxemasi tu'rli paketlerge jetkizedi. Yad paketi tu'rleri paket eki qatarli (dual inline packages DIP), apiwayi qatarli yad modeli (single in-line memory modules SIMM), eki qatarli yad qatarlarin (dual in-line memory modules DIMM) o'z ishine aladi. DIP paket eki kerisinshe islep

*turatug'in ayaqli(nun)bolip keramika ya'ki plastinka materealinan tayarlang'an.(su'wret 3.5).*



*Su'wret 3.5. DIP yadina misal.*

*En' joqari da'rejede birlamshi ha'm ekilemshi yadlardi eki gruppag'a bo'liw mu'mkin: ku'shleniwge baylanisli bolg'an ha'm bolamag'an.*

## ***Juwmaqlaw***

*Usi temada hazirgi ku'nde ko'pshilik inobatsiyalarda paydalanip atirg'an atama, jan'a ornatilg'an sistemag'a ta'rip beriw menen baslanadi. Sonnan son' ornailg'an sistema arxitekturasi haqqinda sistemanin' tu'rli strukturalari ta'repten mag'liwmat beredi. Bul bo'lim sondayaq arxitekturaliq jandasiw ne ushin ornatqan sistemani tu'sindiriw ushin qollanilg'anlig'in ha'm ol jandasiw sistemani tu'sindiriwdi a'piwayilastirg'anlig'I haqqinda mag'liwmat berip o'tilgen.*

*Bug'an qosimsha ra'wishte bul jandasiw ornatilg'an sistema menen ne islew yaki ne isley almasliqti aniqlawg'a xizmet qiladi ha'm platag'a jaylasqan sistemani o'zgartiriw odan qayta paydalaniw imkanyatina alip keledi, bul arqali naq pul pa'seyiwi mu'mkin. Keyingi temada ornatilg'an sistemani proektlestiriwde qanday kerekli rol oynawdi ko'rsetip beriwshi d'slepki real-du'nyadan misallardi o'z ishine aladi. Budan ma'xset a'piwayi qurilmalar menen baylanisli standartlardi biliw ha'm tu'siniwdin kerekli ko'rsetkishi ha;m bul standartlardi jana arxitektura jaratiw ushin qollanadi.*

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